Remarks:

In the present paper, Claims 1-29 are pending. Claim 7 has been amended

35 U.S.C. § 112, second paragraph

Claim 7 stands rejected under 35 U.S.C. §112, second paragraph. The Examiner argues that there is no antecedent support for the recitation of "said data element" as claimed.

Claim 7 has been amended herein to clarify that the queue logic merges a sequence number derived from the count value of the current event counter with each data event stored in the queue. Support for the amendment can be found, for example, on page 21, lines 15-25 of applicants' specification. Moreover, the phrase "said data element" has been canceled from claim 7. In view of the amendments and clarifying comments herein, the applicants respectfully request that the rejection to claim 7, under 35 U.S.C. §112, second paragraph, be withdrawn.

35 U.S.C. § 102(b)

Claims 1-25 and 27-29 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Pat. No. 4,535,420 to Fung (hereinafter, '*Fung*'). According to the M.P.E.P. §706.02, in order to be anticipating under §102, the reference must teach every aspect of the claimed invention[1]. The applicants' respectfully traverse the rejection to each of the above claims under 35 U.S.C. § 102(b). Of the rejected claims, claims 1, 11 and 23 are in independent form.

Independent Claim 1:

With regard to claim 1, the applicants respectfully assert that *Fung* fails to teach or suggest at least:

> A queueing system comprising ... a current event counter updated by said queue logic to keep track of a count value that corresponds to the total number of data events written to said queue, said current event counter capable of counting an amount

[1] See also *Carella v. Starlight Archery and Pro Line Co.*, 804 F.2d 135, 138, 231 U.S.P.Q. 644, 646 (Fed. Cir. 1986).

> that is greater than said plurality of addressable storage locations...

In making the rejection to claim 1, the Examiner argues that the claimed current event counter reads on the disclosed access counter 13 in *Fung*. The Examiner further cites Col. 8, lines 63-65; Col. 2, lines 22-24 and Col. 4, line 38 in the disclosure of *Fung* for further support of the rejection. The applicants' respectfully traverse this interpretation.

Fung discloses a multiplexer (MUX) 11 that is arranged to provide address signals to RAM 10 (on a mutually exclusive basis) from one of an address holding register 12 associated with a microprocessor via bus 21 or an access counter 13, which stores an address associated with the minicomputer 16 via address data and control bus 15[2].

During retrieval of information from RAM 10 to bus 20, the address held in the access counter 13 is compared with an original minicomputer address, which has been previously stored. If the addresses are identical, the information previously fetched from RAM 10 will be considered as valid information. If the addresses are not identical, the RAM 10 will be considered invalid and the RAM data retrieval operation is repeated. This operation continues until the address comparison indicates an identical match. Thus, the access counter 13 simply enables the disclosed memory unit to function as a conventional *dual port memory*[3].

The access counter 13 controls one of two possible sources of *address information* used by the RAM 10 and is utilized to implement a form of dual port memory. However, *Fung* fails to teach or suggest that the access counter 13 implements a current event counter updated by queue logic to keep track of a count value that corresponds to the total number of data events written to the queue as claimed. For example, since the access counter 13 stores an address used

[2] See *Fung*, Col. 2, lines 25-36. In particular, MUX 11 will supply address signals to RAM 10 from the address holding register 12 except when signals are presented by the access counter 13. In this regard, priority is given to the access counter 13 via a PGMIO control signal carried by the address data and control bus 15. See Fung, Col. 3, lines 26-34.

[3] See *Fung*, Col. 3, lines 35-65.

to access the RAM, when the limits of the storage capacity of the RAM have been reached, the address stored by the access counter will merely reset to the next available storage address. That is, the access counter *does not* count events, but rather tracks (and increments) addresses for accessing the RAM.

In this regard, *Fung* is completely silent to the teaching or suggestion of *any* counter that keeps track of a count value that corresponds to the total number of data events written to the queue as claimed. For example, the passage cited by the Examiner at Col. 8, lines 63-65 explicitly states that the counter 13 merely "... provides a pointer to sequentially select the next available location..." in the RAM[4]. Col. 2, lines 22-24 merely gives an exemplary size of the RAM 10 and Col. 4, line 38 illustrates how the total capacity of RAM 10 (e.g., 16x16) can be implemented using multiple physical memory devices, e.g., four 4x16 RAMs that can be combined for the total 16x16 memory.

The above cited passages fail to teach or suggest at least a current event counter updated by said queue logic to keep track of a count value that corresponds to the total number of data events written to said queue as claimed. In view of the clarifying comments herein, the applicants' respectfully request that the rejection of claim 1 under 35 U.S.C. § 102(b) and the claims that depend there from, be withdrawn.

Independent Claim 11:

With regard to claim 11, the applicants respectfully assert that *Fung* fails to teach or suggest at least:

> A queueing system comprising ... an event counter operatively configured to sequentially update a count value stored therein each time a data event is written into said queue, said count value capable of storing a maximum count that exceeds said predetermined number of addresses...

[4] See Fung, Col. 8, lines 63-64.

As claim 11 recites an event counter operatively configured to sequentially update a count value stored therein each time a data event is written into said queue, the arguments in support of claim 1 set out above apply by analogy to claim 11. In view of the clarifying comments herein, the applicants' respectfully request that the rejection of claim 11 under 35 U.S.C. § 102(b) and the claims that depend there from, be withdrawn.

Independent Claim 23:

With regard to claim 23, the applicants respectfully assert that *Fung* fails to teach or suggest at least:

> A method of queuing data comprising ...keeping track of a current count value that corresponds to the total number of data events written to said queue, said current count value capable of counting an amount that is greater than the number of said addressable storage locations ...

As claim 23 recites keeping track of a current count value that corresponds to the total number of data events written to the queue, the arguments in support of claim 1 set out above apply by analogy to claim 23. In view of the clarifying comments herein, the applicants' respectfully request that the rejection of claim 23 under 35 U.S.C. § 102(b) and the claims that depend there from, be withdrawn.

35 U.S.C. § 103

Claim 26 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Fung* in view of U.S. Pat. No. 4,872,110 to Smith *et al.* (hereinafter, '*Smith*'). According to the MPEP §706.02(j), to establish a *prima facie* case of obviousness, the prior art references must teach or suggest all the claim limitations.

The applicants respectfully submit that claim 26 is patentable over *Fung* in view of *Smith* by virtue of being dependent upon claim 23, which the applicants believe to be patentable as described in greater detail herein.

Independent Claim 1 is patentable over Unger in view of Heap:

Claims 1 and 2 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 3,935,563 to Unger (hereinafter, '*Unger*') in view of U.S. Pat. No. 4,231,106 to Heap *et al.* (hereinafter, '*Heap*'). The applicants respectfully traverse this rejection.

With regard to claim 1, the applicants respectfully assert that *Unger* in view of *Heap* fails to teach or suggest at least:

> A queueing system comprising ... a current event counter updated by said queue logic to keep track of a count value that corresponds to the total number of data events written to said queue, said current event counter capable of counting an amount that is greater than said plurality of addressable storage locations...

In making the rejection to claim 1, the Examiner argues that the claimed current event counter reads on the disclosed Readout counter 62 in *Unger* in view of the Abstract of *Heap*. The applicants' respectfully traverse this interpretation.

The Readout counter 62 in *Unger* is used to control an adder that determines the address of the instruction and/or operand reference that is read out from the queue[5]. In particular, the Readout counter 62 is cleared each time data is stored in address 337, when lead 66 is active or when a master clear is active on lead 72. For a first read, the Readout counter 62 has a value of zero (0) and the oldest data is selected via the address determined by the counter 44 and the Readout counter 62. At the end of the read, the Readout counter 62 is incremented. However, after 16 reads, the sequence repeats[6]. Thus, the Readout counter 62 is cleared again. That is, the Readout counter 62 does not keep track of a count value that corresponds to the total number of data events written to the queue as claimed.

[5] See *Unger*, Col. 3, lines 12-14; Col. 3, lines 54-58.
[6] See *Unger*, Col. 4, lines 42-60.

Moreover, *Unger* is completely silent with regard to, and thus fails to teach or suggest any structure that is updated by queue logic to keep track of a count value that corresponds to the total number of data events written to the queue.

Further, the Examiner fails to point to any teaching or suggestion in *Heap* that teaches or suggests a current event counter updated by queue logic to keep track of a count value that corresponds to the total number of data events written to the queue.

In view of the clarifying comments herein, the applicants' respectfully request that the rejection of claims 1 and 2 under 35 U.S.C. § 103(a) as being unpatentable over *Unger* in view of *Heap* be withdrawn.

Independent Claim 1 is patentable over Unger in view of Lindsay:

Claims 1 and 2 also stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Unger* in view of "A Hardware Monitor Study of a CDC KRONOS System" by Lindsay (hereinafter, 'Lindsay'). The applicants respectfully traverse this rejection.

With regard to claim 1, the applicants respectfully assert that *Unger* in view of *Lindsay* fails to teach or suggest at least:

> A queueing system comprising ... a current event counter updated by said queue logic to keep track of a count value that corresponds to the total number of data events written to said queue, said current event counter capable of counting an amount that is greater than said plurality of addressable storage locations...

The teaching of Unger is already described herein. Moreover, the Examiner fails to point to any teaching or suggestion in *Lindsay* that teaches or suggests a current event counter updated by queue logic to keep track of a count value that corresponds to the total number of data events written to the queue.

In view of the clarifying comments herein, the applicants' respectfully request that the rejection of claims 1 and 2 under 35 U.S.C. § 103(a) as being unpatentable over *Unger* in view of *Lindsay* be withdrawn.

CONCLUSION

For all of the above reasons, it is respectfully submitted that the above claims recite allowable subject matter. The Examiner is encouraged to contact the undersigned attorney to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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